REMARKS/ARGUMENTS

Claims 1-18 are pending in the subject application and each has been rejected in the October 30, 2007 Office action. No claim amendments are filed herein.

This response is filed further to Applicants' previous Response of December 27, 2007, and responsive to the January 17, 2008 Advisory Action. Applicants take this opportunity to thank Examiner Pompey for discussing the Advisory Action in a brief telephone conversation with Applicants' undersigned representative that took place on January 31, 2008.

Applicants respectfully request reconsideration and allowance of each of pending claims 1-18.

I. Rejection of Claims 1, 3-5, 9, 14-15, 17 and 18 under 35 U.S.C. § 103

In paragraph 2 of the October 30, 2007 Office action, claims 1, 3-5, 9 and 14-15, 17 and 18 were rejected under 35 U.S.C § 103(a) as being unpatentable over Clark et al. (U.S. Pat. No. 6,767,793), hereinafter "Clark" in view of Fried et al, (USPUB 2003/0113970), hereinafter "Fried." Applicants respectfully submit that these claim rejections should be withdrawn for reasons set forth below.

Each of independent claims 1 and 17 provides a gate electrode over the top of a semiconductor fin device. In particular, each claim recites a fin device with a thin film gate dielectric formed on the top and the opposed sides of the fin. Each claim also recites a gate electrode material formed over the top and sides of the fin to form a single transistor with a channel extending along the sides and top of the fin.

In particular, claim 1 recites the feature of:

> a substantially planar surface formed only of a gate electrode material disposed atop the semiconductor device and extending distally past each of the opposed sides.

Claim 17 recites the feature of:

> gate electrode formed of a layer of gate electrode material and having a substantially planar surface disposed atop the gate dielectric film formed over the fin and extending distally past each of the opposed sides of the fin.

In each claim, the gate electrode material with a planar upper surface extends past the opposed sides of the fin device and above the top of the fin device. Because the gate electrode material is formed over and extending past the opposed sides of the fin device coated with a gate dielectric on its top and opposed sides, each of claims 1 and 17 also provide:

> "the top and the opposed sides of the semiconductor device each form a channel portion of a **single** associated **transistor**."

The claimed invention of claims 1 and 17 is therefore distinguished from the **Clark** reference because, in the Clark reference, gate electrode material does not extend over the top of the alleged fin.

The claimed invention of claims 1 and 17 is also distinguished from the **Fried** reference because, in the Fried reference, there is no channel, no gate dielectric, and no gate electrode material formed on the top of the alleged fin and because two distinct transistors are formed on opposed sides of the fin.

In the October 30, 2007 Office action, on page 2, the Examiner alleges that Clark discloses "*wherein the semiconductor device comprises a semiconductor fin (300, fig. 31) with a planar top surface and the top and the opposed sides of the semiconductor device each form a channel portion . . . .*" Applicants respectfully disagree and point out that the top of the fin in Clark does NOT form a channel portion because there is no gate electrode over the top of Clark's semiconductor fin as would be required to form a channel and therefore the top of the semiconductor device, i.e. the semiconductor fin, cannot and does not form a channel portion of any transistor.

The Examiner then refers to the Fried reference and alleges feature 32 of fig. 5B to be the gate electrode material, in both the October 30, 2007 Office Action and in the Advisory Action, in which the Examiner provides:

> However, when forming a gate electrode (32, fig. 5B of Fried) to replace the gate electrode 310, fig. 31), a channel will exist on the sides and top of the fin as claimed. Fried is only being used to show how one of ordinary skill in the art would form a gate electrode over a fin structure.

In response to this assertion by the Examiner, Applicants respond as follows.

1) Clark does not provide the advantage of a single transistor having an extended channel that extends <u>both</u> along the opposed sides and also along the top of a semiconductor fin, because Clark does not provide a gate electrode over top of the semiconductor fin. This "no gate electrode over top" deficiency of Clark does not appear to be controverted by the Examiner, although the Examiner does apparently contend that there exists a channel on top of the fin, as discussed supra.

2) Clark provides no intention or suggestion to form a gate electrode over the semiconductor fin device. In column 7, lines 58-63, Clark provides: *However, in a different embodiment, the gate electrodes 310 can be made asymmetric with, for example, an ion implant to result in an asymmetric gate workfunction Fin FET with strain. More specifically, in the asymmetric gate arrangement, the gate conductors 310 would have different dopant concentrations or utilize different dopants.* In order to provide this option of having differently doped gate electrodes forming transistors with different operating characteristics on opposed sides of the fin, Clark surely is not contemplating a single transistor on both sides and over top of the fin. The *absence* of a gate electrode over top of the fin allows for this option and the presence of a single gate electrode over the top and sides of the fin, would preclude this option. This teaching would therefore <u>discourage</u> one of ordinary skill from using a single gate electrode material extending over top and past both sides of the semiconductor fin.

Clark, therefore, *teaches away* from adding a gate electrode over top of the semiconductor device.

3) Notwithstanding the foregoing, Fried does **not** teach providing a **gate electrode** that extends over top and past both sides of a semiconductor fin device such that the gate electrode forms channels of a transistor on top of the fin, much less channels of the same transistor on the opposed sides and over top of the semiconductor fin. The feature referred to by the Examiner – feature 32 – is a polysilicon-containing or metal interconnect layer formed over a metallic layer 30 and serves as a contact/interconnect device – not a gate electrode. Applicants acknowledge that planarization techniques, such as the planarization of this interconnect layer taught by Fried and offered by the Examiner, are known in the art. What Fried fails to provide, however, is the use of a gate electrode material, planarized or unplanarized, that extends both over the top and past the opposed sides of a subjacent semiconductor fin.

As indicated by the title, Implanted Asymmetric Doped Polysilicon Gate FINFET, Fried is directed to forming two different gate portions on opposed sides of a fin, not a singular transistor with a channel that extends along both sides of a fin as well as over the top. As in the abstract of Fried, the asymmetric FET includes a p-type gate portion and an n-type gate portion on a vertical semiconductor body and; "an interconnect between the p-type gate portion and the n-type gate portion," NOT a gate electrode material. Throughout the Fried disclosure, it is clear that semiconductor structures 24, 26 form the p-type and n-type gate electrode portions and that the channel portions opposite the respective p-type and n-type electrodes do not form the same channel of a single transistor. Moreover, hard mask 14 which is disposed atop the semiconductor fin prevents ANY material formed over the semiconductor fin device 12, from acting as a gate electrode and prevents the top of the fin from being a transistor channel. Semiconductor device 26 is an n- gate device and semiconductor device 24 is a p- gate device in the asymmetric FET device. These are not sections of a single transistor.

Again, while Applicants acknowledge that Fried provides a planarizing process, Applicants respectfully submit that Fried does not provide forming a gate electrode that extends past both sides and over the top of a subjacent semiconductor fin. Moreover, Fried does not support this feature simply because a planarization technique is disclosed.

In summary, neither of the references nor the combination thereof, provides the claimed features of a fin with a gate dielectric that extends along the sides and over the top of the fin and a gate electrode material with a planar top surface that is formed over and along opposed sides of, the fin providing a single transistor with a channel extending along the opposed sides and along the top of the fin.

Independent claims 1 and 17 are therefore distinguished from the references of Clark and Fried, taken alone or in combination. The rejection of claims 1, 3-5, 9, 14-15, 17 and 18 in this section should be withdrawn because claims 3-5, 9 and 14-15 depend from claim 1 and also because claim 18 depends from claim 17.

II. Rejection of Dependent Claims 2, 6-8, 10-13 and 16-17

In paragraphs 4-6 of the subject Office action, claims 2, 6-8, 10-13 and 16-17 were variously rejected under 35 U.S.C § 103(a) as being unpatentable over Clark in view of Fried, and further in view of tertiary references of Kinsbron (U.S. Pat. No. 4,432,132), Fried et al. (USP 6,657,252), hereinafter "Fried II", and Achuthan, et al. (U.S. 6,855,607). Applicants respectfully submit that these claim rejections are overcome because each of these claims depends from claim 1 which is distinguished from Clark in view of Fried and because Kinsbron, Fried II and Achuthan et al., do not make up for the above-stated deficiencies of Clark and Fried for reasons stated in the December 27, 2007 Response.

As such, the rejection of claims 2, 6-8, 10-13 and 16-17 under 35 U.S.C. § 103(a), should be withdrawn.

CONCLUSION

Based on the foregoing, Applicants respectfully submit that each of claims 1-18 is in allowable form and the application is therefore in condition for allowance, which action is expeditiously and respectfully requested by Applicants.

The Assistant Commissioner for Patents is hereby authorized to charge any fees or credit any excess payment that may associated with this communication, to Deposit Account 04-1679.

Respectfully submitted,

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